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use Constants and

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 VHDL consists of a
 design entity that can
 contain other entities
 that are then
 considered
 components of the top-
 level entity. Each entity
 is modeled by an entity
 declaration and an
 architecture body. One
 can consider the entity
 declaration as the
 interface to the outside

world that defines the input and output signals, while

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Contents Preface vi
CHAPTER 1.
Introduction 1 1.1.
What is VHDL? 1 1.2.
History 1 1.3.
Capabilities 1 1.4.
Hardware Abstraction 2
CHAPTER 2. A Tutorial
4 2.1. Basic
Terminology 4 2.2 ...

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verbose language with
many complex
constructs that have
complex semantic
meanings and is
initially difficult to
understand (the US
military requires VHDL
for device designs,
thus explains its
popularity vs. other
HDLs).

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VHDL program (code)
is used to implement
digital circuit inside
CPLD / FPGA, or it can
be used to fabricate
ASIC (Application

Specific Integrated
Circuit) It is very useful
in developing high end,
sophisticated
microprocessor or
micro-controller like
ASIP (Application
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(Programmable System
on Chip)

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idea that the designer
of the circuit needs a
simple way to describe
the components of a
circuit in software. §
There are several basic
primitive gates that are
built into Verilog. ú
two-input gates shown
here, but multi-input
also possible. Ø
and(out,in,in) Ø
or(out,in,in) Ø
not(out,in)

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